respect to pixels arranged in columns and rows of an array of a display device, comprising:

a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal;

a control bus coupled to said first terminal of each of said plurality of semiconductor switches for communicating corresponding signals; and

a plurality of local buses that are separated from one another for communicating corresponding signals, a given one of said plurality of local buses having a first bus section coupled to said second terminal of respective ones of said plurality of semiconductor switches, each said first bus section extending in a manner to cross said control bus and a second bus section connected to said first bus section and having conductors thereof coupled to the second terminals of the respective ones of said plurality of switches, the associated switches having the third terminals thereof coupled to the consecutively disposed column conductors of the array of the display device.

B6 cont.

2. (Amended) An arrangement according to Claim 1 wherein said first plurality of terminals receive switch control signals and said second plurality of terminals receive picture information signals for said switches for storing the picture information in said pixels of said array.

3. (Amended) An arrangement according to Claim 1 wherein said associated switches including a plurality of sub-groups of switches, the switches of a given sub-group having the first terminals thereof coupled in common to a corresponding conductor of said first bus and the third terminals thereof being coupled to consecutively disposed column conductors, respectively, of said array.

4. (Amended) An arrangement according to Claim 1 wherein the conductors of said second bus section of said given local bus are disposed proximate said switches associated with said given bus and remote from switches associated with the other local buses of said plurality of local buses to provide bus separation.

5. (Amended) An arrangement according to Claim 1 wherein the conductors of said first bus extend along each of said plurality of semiconductor switches to form a global bus arrangement.

7. (Amended) A signal demultiplexer for a display panel, comprising:

a plurality of switch groups, each switch group having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each group connected to a common control terminal, and having respective output terminals coupled to successive data lines on the display panel;

a plurality of groups of data buses, each group of data buses having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective groups of data buses being coupled to input terminals of corresponding ordinally numbered switches of a plurality of said switch groups;

a control bus including a plurality of conductors, said control bus arranged to cross said plurality of groups of data buses; and

connections between ones of said plurality of conductors of said control bus and respective common control terminals of said clusters of switches.

8. (Amended) A signal demultiplexer for a display panel, comprising:

a plurality of switch groups, a given switch group having ordinally numbered switches arranged sequentially, and each switch having respective input, output and control terminals, the output terminals coupled to successive data lines on the display panel;

a group of data buses, a given data bus thereof having ordinally numbered conductors arranged sequentially, a given conductor of said given data bus being coupled in common to the input terminal of each switch having the same ordinal number that corresponds to the ordinal number of said given conductor and being included in each switch group associated with said given data bus;

a control bus including a plurality of conductors, said control bus arranged to cross said group of data buses; and

connections between ones of said plurality of conductors of said control bus and respective control terminals of said switch groups.

B7 cont. 9. (Amended) A signal demultiplexer according to Claim 8 wherein the control terminals of all the switches in each cluster of switches are connected in common to a corresponding conductor of said control bus.